In the Claims

Please delete Claims 4, 8, and 10-22 without prejudice, add new Claims 23-24, and amend the remaining claims as follows:

1. (currently amended) A fused Booth encoder multiplexer logic cell comprising:

a logic circuit having a plurality of operand input bits including multiplier input bits and multiplicand input bits, and an output node which produces a single partial product bit according to a Boolean function of said plurality of operand input bits based on a Booth encoding and selection algorithm, wherein the logic circuit includes

a clock input;

a logic tree containing a plurality of logic transistors controlled respectively by said plurality of operand bit inputs and interconnected to carry out the Boolean function to produce a value for a multiplication operation at a dynamic node, said logic tree including a plurality of transistor stacks, each transistor stack having a plurality of said logic transistors serially connected source-to-drain, with one logic transistor in each stack having a source connected to said drain of power transistor and said dynamic node, and another logic transistor in each stack having a drain connected to said source of said foot transistor, wherein said operand bit inputs include a plurality of multiplicand bit inputs and a plurality of multiplier bit inputs, and a given one of said transistor stacks includes a first logic transistor having a gate controlled by one of said multiplicand bit inputs, a second logic transistor having a gate controlled by a first one of said multiplier bit inputs, a third logic transistor having a gate controlled by a second one of said multiplier bit inputs, and a fourth logic transistor having a gate controlled by a third one of said multiplier bit inputs;

a power transistor coupling said logic tree to a voltage source, said power transistor being controlled by said clock input;

a foot transistor coupling said logic tree to electrical ground, said foot transistor being controlled by said clock input; and

a latch connected to said dynamic node which maintains the value at said output node, said latch being controlled by said clock input.

2. (original) A fused Booth encoder multiplexer utilizing a plurality of fused Booth encoder multiplexer logic cells according to Claim 1, wherein:

the logic cells are arranged in a two-dimensional array on an integrated circuit and operate in parallel to produce a respective plurality of partial product bits; and

a given one of the logic cells has a unique set of multiplicand and multiplier input bits.

3. (original) The fused Booth encoder multiplexer logic cell of Claim 1 wherein:

the operand inputs bits include two multiplicand input bits A(i..i+1) and three multiplier input bits C(i-1..i+1); and

the Boolean function which produces the single partial product bit is given by the expression

$$S = (A(i) \oplus C(i-1)) \cdot (C(i) \oplus C(i+1)) + A(i+1) \cdot \overline{C(i-1)} \cdot C(i) \cdot C(i+1) + \overline{A(i+1)} \cdot C(i-1) \cdot \overline{C(i)} \cdot \overline{C(i+1)}.$$

4. (canceled)

5. (currently amended) The fused Booth encoder multiplexer logic cell of Claim [[4]] 1 wherein said latch includes:

a first P-MOS transistor having a drain connected to said dynamic node, a source connected to said voltage source, and a gate;

a second P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain connected to said gate of said first P-MOS transistor and said output node; and

an N-MOS transistor having a gate connected to said dynamic node, a source connected to said drain of said second P-MOS transistor, said gate of said first P-MOS transistor and said output node, and a drain connected to electrical ground.

6. (currently amended) The fused Booth encoder multiplexer logic cell of Claim [[4]] 1 wherein said latch includes:

a first P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain;

a second P-MOS transistor having a gate, a source connected to said voltage source, and a drain connected to said drain of said first P-MOS transistor;

a first N-MOS transistor having a gate connected to said dynamic node, a source connected to said drains of said first and second P-MOS transistors, and a drain;

a second N-MOS transistor having a gate connected to said clock input, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground;

a third N-MOS transistor having a gate, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground; and

an inverter having an input connected to said drains of said first and second P-MOS transistors, and an output connected to said gates of said first P-MOS transistor and said third N-MOS transistor, said inverter output being further connected to said output node to produce an inverted value.

7. (original) The fused Booth encoder multiplexer logic cell of Claim 6 wherein said first P-MOS transistor and said first N-MOS transistor invert the value from the dynamic node, and the Boolean function of said logic tree accounts for inversion of the value by said first P-MOS transistor and said first N-MOS transistor.

8. (canceled)

9. (currently amended) The fused Booth encoder multiplexer logic cell of Claim ~~8~~ 1 wherein a first source/drain junction in a first one of said transistor stacks is connected to a second source/drain junction in a second one of said transistor stacks.

10. – 22. (canceled)

23. (new) A fused Booth encoder multiplexer logic cell comprising:

a logic circuit having a plurality of operand input bits including multiplier input bits and multiplicand input bits, and an output node which produces a single partial product bit according to a Boolean function of said plurality of operand input bits based on a Booth encoding and selection algorithm, wherein the logic circuit includes

a clock input;

a logic tree containing a plurality of logic transistors controlled respectively by said plurality of operand bit inputs and interconnected to carry out the Boolean function to produce a value for a multiplication operation at a dynamic node;

a power transistor coupling said logic tree to a voltage source, said power transistor being controlled by said clock input;

a foot transistor coupling said logic tree to electrical ground, said foot transistor being controlled by said clock input; and

a latch connected to said dynamic node which maintains the value at said output node, said latch being controlled by said clock input and including a first P-MOS transistor having a drain connected to said dynamic node, a source connected to said voltage source, and a gate, a second P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain connected to said gate of said first P-MOS transistor and said output node, and an N-MOS transistor having a gate connected to said dynamic node, a source connected to said drain of said second P-MOS transistor, said gate of said first P-MOS transistor and said output node, and a drain connected to electrical ground.

24. (new) A fused Booth encoder multiplexer logic cell comprising:

a logic circuit having a plurality of operand input bits including multiplier input bits and multiplicand input bits, and an output node which produces a single partial product bit according to a Boolean function of said plurality of operand input bits

based on a Booth encoding and selection algorithm, wherein the logic circuit includes

a clock input;

a logic tree containing a plurality of logic transistors controlled respectively by said plurality of operand bit inputs and interconnected to carry out the Boolean function to produce a value for a multiplication operation at a dynamic node;

a power transistor coupling said logic tree to a voltage source, said power transistor being controlled by said clock input;

a foot transistor coupling said logic tree to electrical ground, said foot transistor being controlled by said clock input; and

a latch connected to said dynamic node which maintains the value at said output node, said latch being controlled by said clock input and including a first P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain, a second P-MOS transistor having a gate, a source connected to said voltage source, and a drain connected to said drain of said first P-MOS transistor, a first N-MOS transistor having a gate connected to said dynamic node, a source connected to said drains of said first and second P-MOS transistors, and a drain, a second N-MOS transistor having a gate connected to said clock input, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground, a third N-MOS transistor having a gate, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground, and an inverter having an input connected to said drains of said first and second P-MOS transistors, and an output connected to said gates of said first P-MOS transistor and said third N-MOS transistor, said inverter output being further connected to said output node to produce an inverted value.